



TFT LCD Tentative Specification

MODEL NO.: V420H2 – LE4

Customer: _____

Approved by: _____

Note:

Approved By	TV Head Division	
	Chao-Chun Chung	

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Ken Wu	Peggi Chiu



- CONTENTS -

REVISION HISTORY	3
1. GENERAL DESCRIPTION	4
1.1 OVERVIEW	
1.2 FEATURES	
1.3 APPLICATION	
1.4 GENERAL SPECIFICATIONS	
1.5 MECHANICAL SPECIFICATIONS	
2. ABSOLUTE MAXIMUM RATINGS	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	
2.2 PACKAGE STORAGE	
2.3 ELECTRICAL ABSOLUTE RATINGS	
2.3.1 TFT LCD MODULE	
2.3.2 BACKLIGHT UNIT	
3. ELECTRICAL CHARACTERISTICS	7
3.1 TFT LCD MODULE	
3.2 BACKLIGHT CONVERTER UNIT	
3.2.1 LED LIGHT BARCHARACTERISTICS	
3.2.2 CONVERTER CHARACTERISTICS	
3.2.3 CONVERTER INTERFACE CHARACTERISTICS	
4. BLOCK DIAGRAM	13
4.1 TFT LCD MODULE	
5. INTERFACE PIN CONNECTION	14
5.1 TFT LCD MODULE	
5.2 BACKLIGHT UNIT	
5.3 CONVERTER UNIT	
5.4 BLOCK DIAGRAM OF INTERFACE	
5.5 LVDS INTERFACE	
5.6 COLOR DATA INPUT ASSIGNMENT	
6. INTERFACE TIMING	25
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	
6.2 POWER ON/OFF SEQUENCE	
7. OPTICAL CHARACTERISTICS	28
7.1 TEST CONDITIONS	
7.2 OPTICAL SPECIFICATIONS	
8. DEFINITION OF LABELS	32
8.1 CMO MODULE LABEL	
9. PACKAGING	33
9.1 PACKING SPECIFICATIONS	
9.2 PACKING METHOD	
10. PRECAUTIONS	35
10.1 ASSEMBLY AND HANDLING PRECAUTIONS	
10.2 SAFETY PRECAUTIONS	
11. MECHANICAL CHARACTERISTICS	36

**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 0.0	Mar 11,10'	All	All	Tentative Specification was first issued.
Ver 0.1	Mar 25,10'	10	3.2	Backlight Converter Unit
Ver 0.1	Mar 25,10'	29	7.2	Optical Specifications

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H2- LE4 is a 42" TFT Liquid Crystal Display module with LED Backlight and 2 ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness (450 nits)
- Ultra-high contrast ratio (6000:1)
- Faster response time (gray to gray average 4.5 ms) (5.5ms)
- High color saturation NTSC 72% (70%)
- Ultra wide viewing angle : 176(H)/176(V) (CR \geq 20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24 (H) x 523.26 (V) (42" diagonal)	mm	(1)
Bezel Opening Area	937.24 (H) x 530.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally Black	-	
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	-	973.24	-	mm	(1)
	Vertical(V)	-	566.26	-	mm	(1)
	Depth(D)	-	10.8	-	mm	
	Depth(D)	24.6	25.6	26.6	mm	To converter cover
Weight			7950			

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

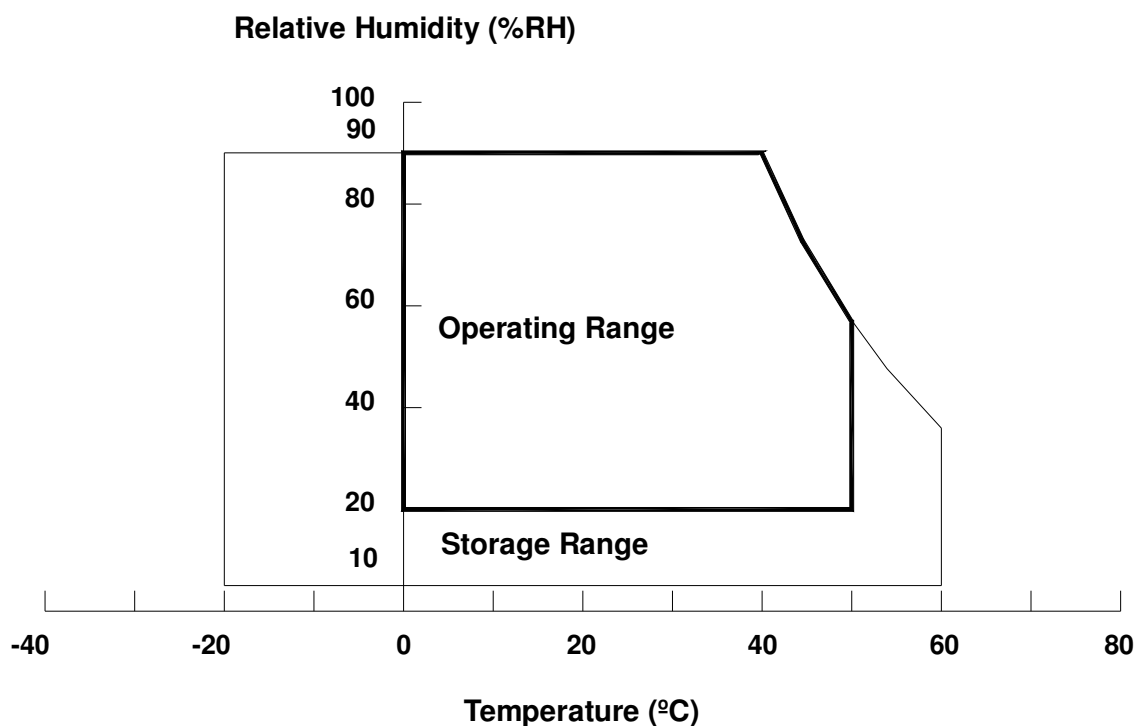
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.





2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	13.5	V	
Input Signal Voltage	V _{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V _W	Ta = 25 °C	-	-	60	V _{RMS}	
Converter Input Voltage	V _{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

3. ELECTRICAL CHARACTERISTICS

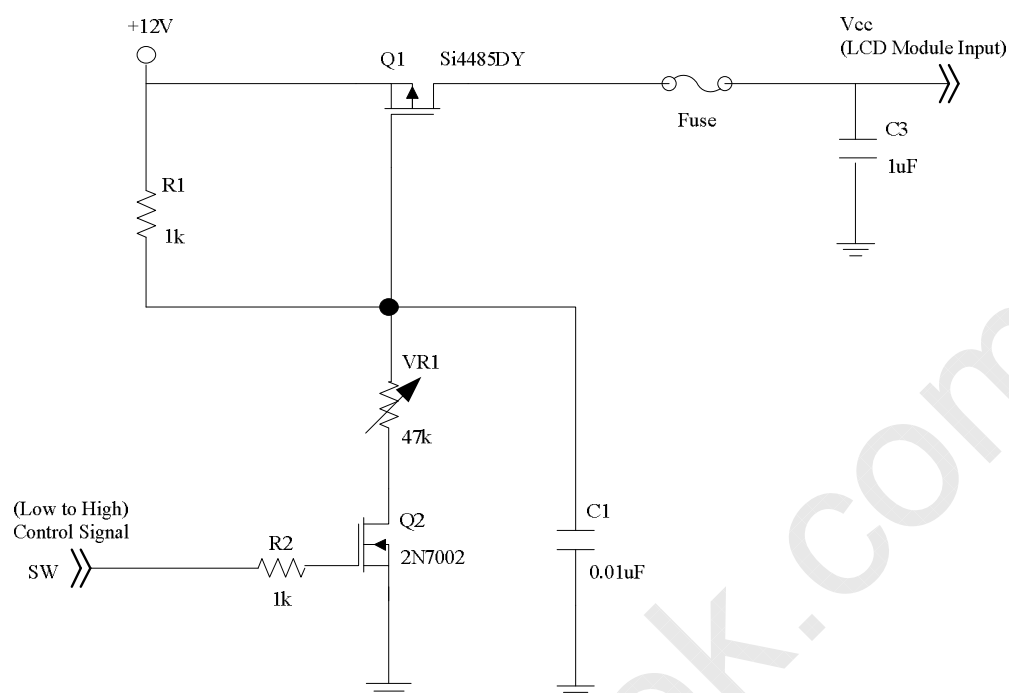
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

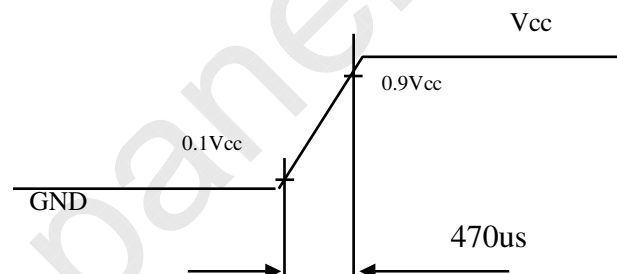
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	-	-	4.2	A	(2)
Power Supply Current	White Pattern	-	-	1.81		A	(3)
	Horizontal Stripe	-	-	1.54		A	
	Black Pattern	-	-	0.58	-	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	-	-	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	-	600	mV	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{cc} = 12V$, $T_a = 25 \pm 2^\circ C$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



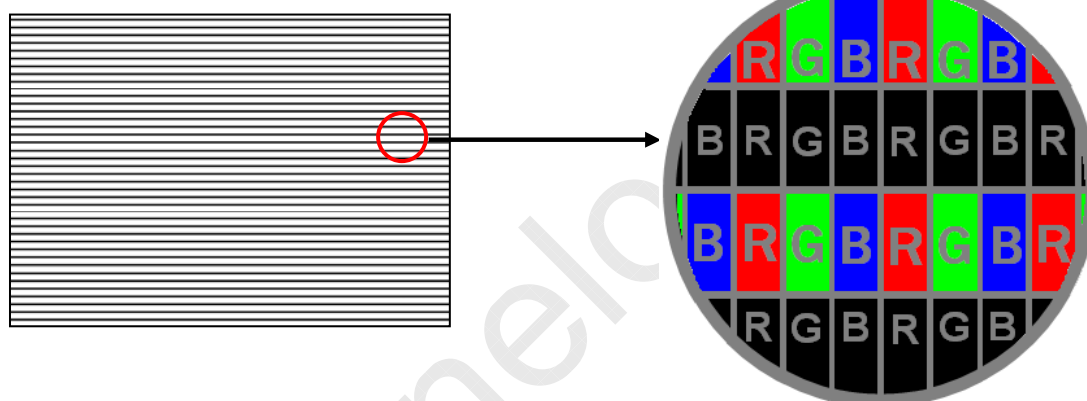
Active Area

b. Black Pattern

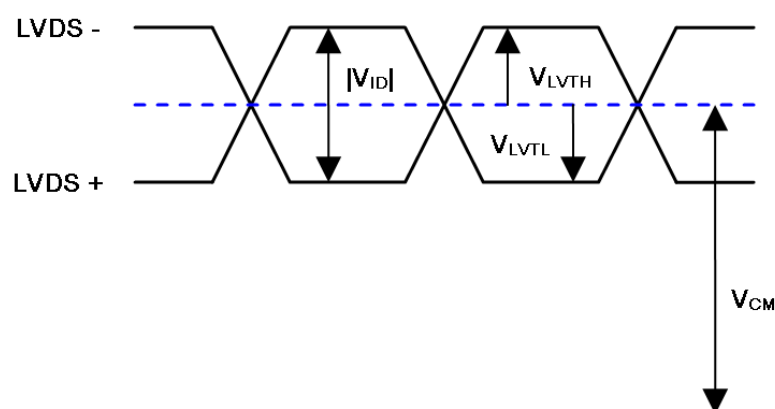


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT CONVERTER UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V _W	-	-	47.6	V _{RMS}	I _L =80 mA
LED Forward Voltage	V _f	3.0	-	3.4	V _{RMS}	I _L =80mA
LED Current	I _L	75.2	80	84.8	mA	

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	TBD	86	W	
Converter Input Voltage	V _{BL}	22.8	24	25.2	V _{DC}	
Converter Input Current	I _{BL}	-	TBD	3.6	A	
Dimming Frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	5	10	-	%	(1)

Note (1) 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

External dimming: 150Hz~170Hz, duty ratio: 10%~100%

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.15	—	3.45	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	
PWM Delay Time		TPWM	—	100	—	—	ms	
BLON Delay Time	T _{on}		—	300	—	—	ms	
	T _{on1}		—	300	—	—	ms	
BLON Off Time		Toff	—	300	—	—	ms	

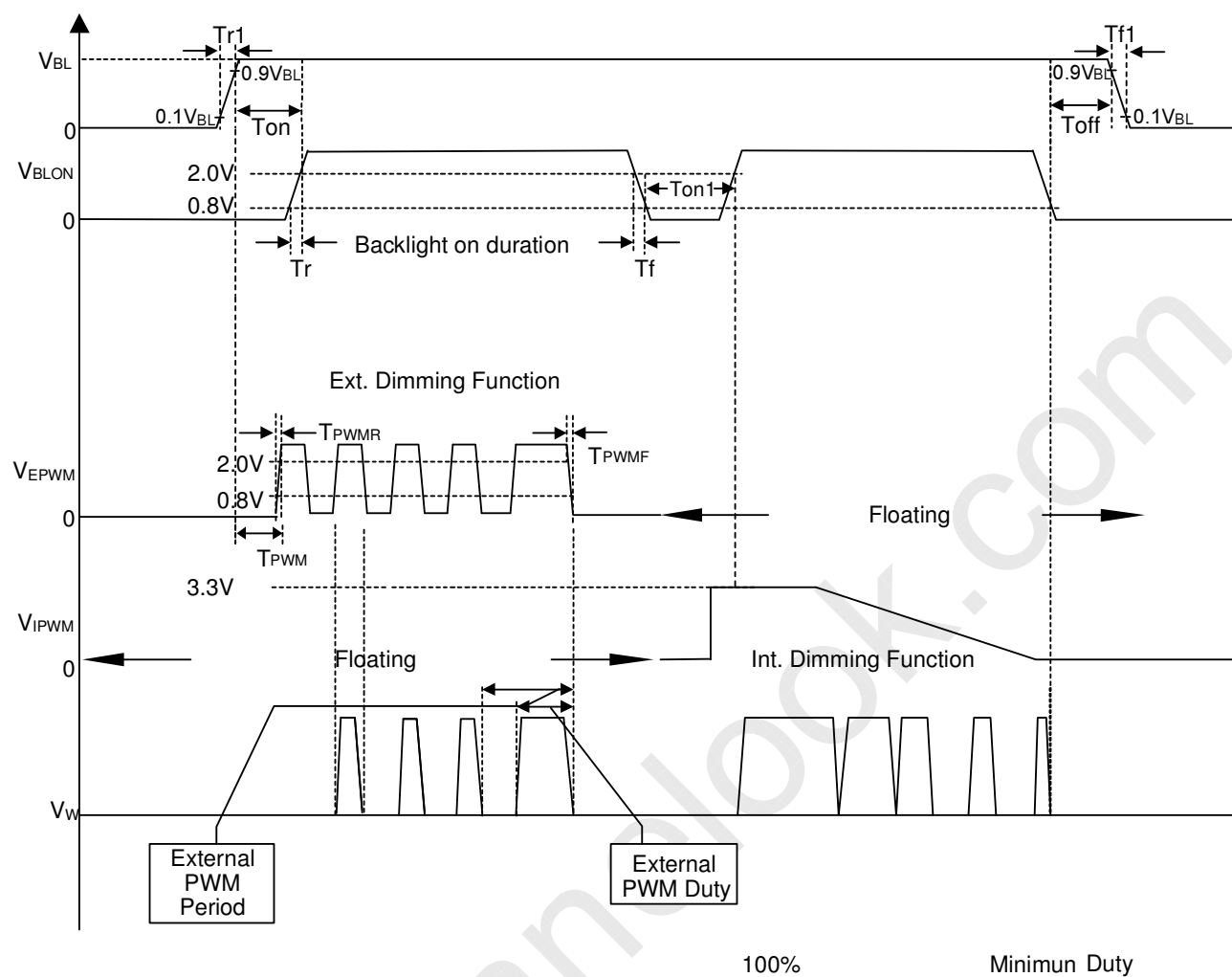
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

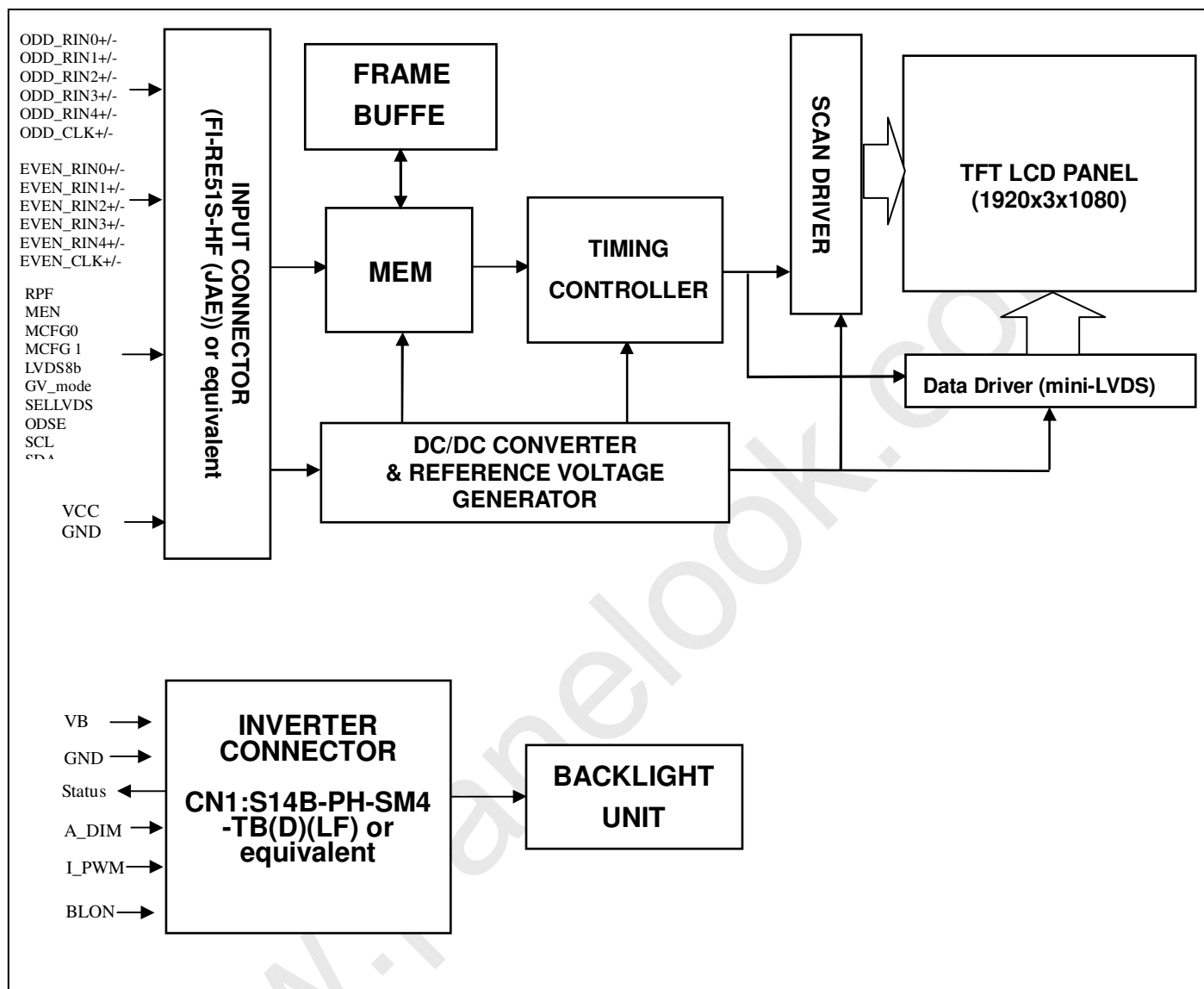
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

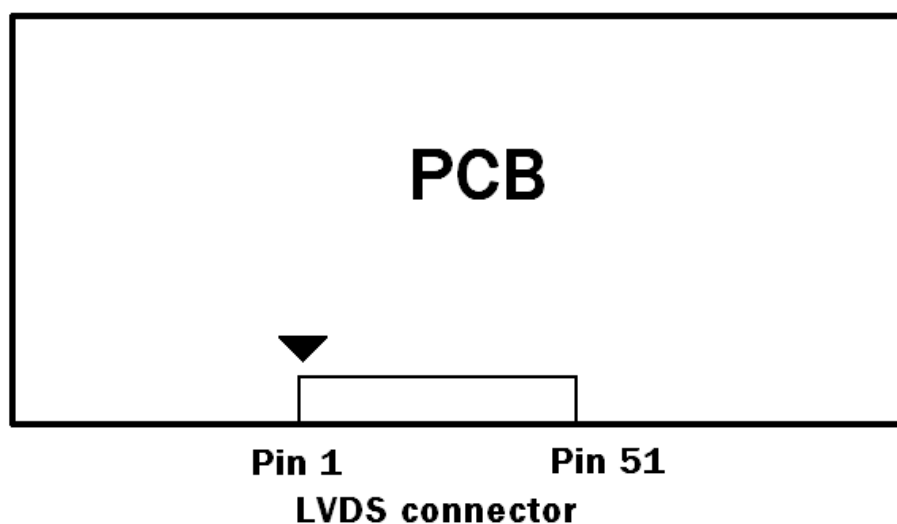
5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment: (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	RPF	Reverse picture function (default low)	8
2	MEN	MEMC function selection	5
3	MCFG0	MEMC function selection	5
4	MCFG1	MEMC function selection	5
5	LVDS8b	8bit/10bit LVDS input selection	6
6	GV_mode	Graphic / Video mode selection	7
7	SELLVDS	LVDS data format Selection	3
8	SCL	I2C CLK Signal	
9	SDA	I2C Data Signal	
10	ODSEL	Overdrive Lookup Table Selection	4
11	GND	Ground	
12	ERX0-	2nd pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	2nd pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	2nd pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	2nd pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	2nd pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	2nd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	2nd pixel Negative LVDS differential clock input.	
20	ECLK+	2nd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	2nd pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	2nd pixel Positive LVDS differential data input. Channel 3	
24	ERX4-	2nd pixel Negative LVDS differential data input. Channel 4	
25	ERX4+	2nd pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	2
27	N.C.	No Connection	2
28	ORX0-	1st pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	1st pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	1st pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	1st pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	1st pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	1st pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	1st pixel Negative LVDS differential clock input.	
36	OCLK+	1st pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ORX3-	1st pixel Negative LVDS differential data input. Channel 3	
39	ORX3+	1st pixel Positive LVDS differential data input. Channel 3	
40	ORX4-	1st pixel Negative LVDS differential data input. Channel 4	

41	ORX4+	1st pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	2
43	N.C.	No Connection	2
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	2
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) LVDS connector pin order defined as follows



Note (2) Reserved for internal use. Please leave it open.

Note (3)

SELLVDS	Mode
L(default)	VESA
H	JEIDA

L: Connect to GND, H: Connect to +3.3V

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Description
L(default)	Lookup table was optimized for 60 Hz frame rate input.
H	Lookup table was optimized for 50 Hz frame rate input.

L: Connect to GND, H: Connect to +3.3V

Note (5) Motion Engine (ME) Level & Demo Function Table

Motion engine level must be adjusted after video mode is selected (or entered).

Adjusting the motion engine level in graphic mode has no effect

		MEN	MCFG1	MCFG0	Notes		
Blanking	Blanking disable	0	0	0	(a)		
	Auto blanking	0	0	1	(b)		
	Blanking enable	0	1	0	(c)		
Effect of ME →				De blur	De judder	Halo	
Demo mode (d)		0	1	1	Demo Window		
ME Level	Strong	1	0	0	Enable	Strong	Strong
	Medium(Default t)	1	0	1	Enable	Normal	Normal
	Weak	1	1	0	Enable	Weak	×
	OFF	1	1	1	×	×	×
		(e) (f) (g)					

(a) Module re-starts processing video signals from Frontend scaler control board.

(b) During sync unstable period such as format change, 60Hz <-> 50Hz .

MCFG0 can be used to insert blanking of 500ms. This signal is toggled.

(c) Module continues to insert blanking until blanking disable signal is received from frontend scaler board.

(d) Demo window mode: Demo Window appears to the left half of display area. Left side with frame is 120Hz with MEMC, and right side is 120Hz w/o motion compensation.

(e) GPIO (General Purpose I/O) sequence of ME Level: (1) MEN; (2) MCFG1; (3) MCFG0.

GPIO sequence of Blanking Enable, Blanking Disable and Demo window: (1) MCFG1; (2) MCFG0; (3) MEN.

(f) Each scaler command must be maintained the same voltage level at least 100ms.

(g) 0 : Connect to GND, 1 : +3.3V

Note (6) 8bit/10bit LVDS input selection

LVDS8b	Bit depth
H(default)	8bit
L	10bit

L : Connect to GND, H : Connect to +3.3V

Note (7) Graphic / Video mode selection

There is no prohibited time period for switching between Graphic mode and Video mode.

When this switching signal is input, LCD will be reset and will re-start selected mode.

GV_mode	Mode select	MEMC ON/OFF
H(default)	Graphic mode	MEMC OFF
L	Video mode	MEMC ON

L : Connect to GND, H : Connect to +3.3V

Note (8)

SELLVDS	Mode
L(default)	Normal Display
H	Rotation Display

L: Connect to GND, H: Connect to +3.3V



5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN7 (Housing): 51281-1094 (Molex)

Pin No.	Symbol	Description
1	VLED	Positive of LED String
2	VLED	
3	NC	No Connection
4	NC	
5	NC	
6	N1	Negative of LED String
7	N2	
8	N3	
9	N4	
10	N5	

Note (1) The backlight interface housing for high voltage side is a model 51281-0994, manufactured by Molex or equivalent. The mating header on converter part number is 51281-0994

5.3 CONVERTER UNIT

CN1(Header): S14B-PH-SM3-TB (JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal (0V)
12	E_PWM	External PWM control signal
13	I_PWM	Internal PWM control signal
14	BLON	Backlight on/off control

Notice:

#PIN 12:PWM Dimming Control (Use Pin 12) : Pin 13 must open.

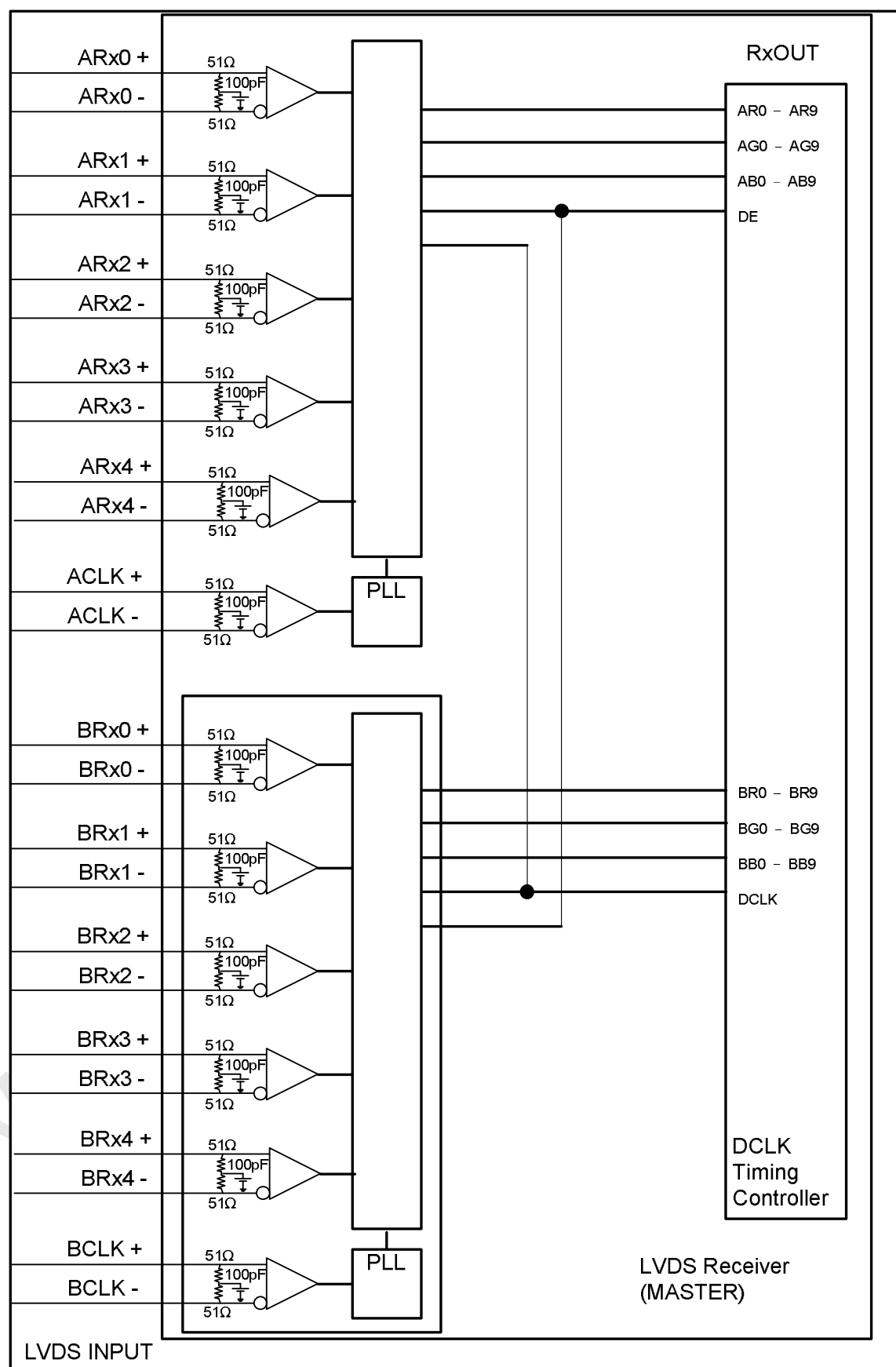
#PIN 13:Analog Dimming Control (Use Pin 13) : 0V~3.3V and Pin 12 must open.

#Pin 13(I_PWM) and Pin 12(E_PWM) can not open in same period.

CN2 ~ CN5 : 51281-1094 (Molex)

Pin №	Symbol	Feature
1	VLED5-	Negative of LED String
2	VLED4-	
3	VLED3-	
4	VLED2-	
5	VLED1-	
6	NC	No Connection
7	NC	
8	NC	
9	VLED+	Positive of LED String
10	VLED+	

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

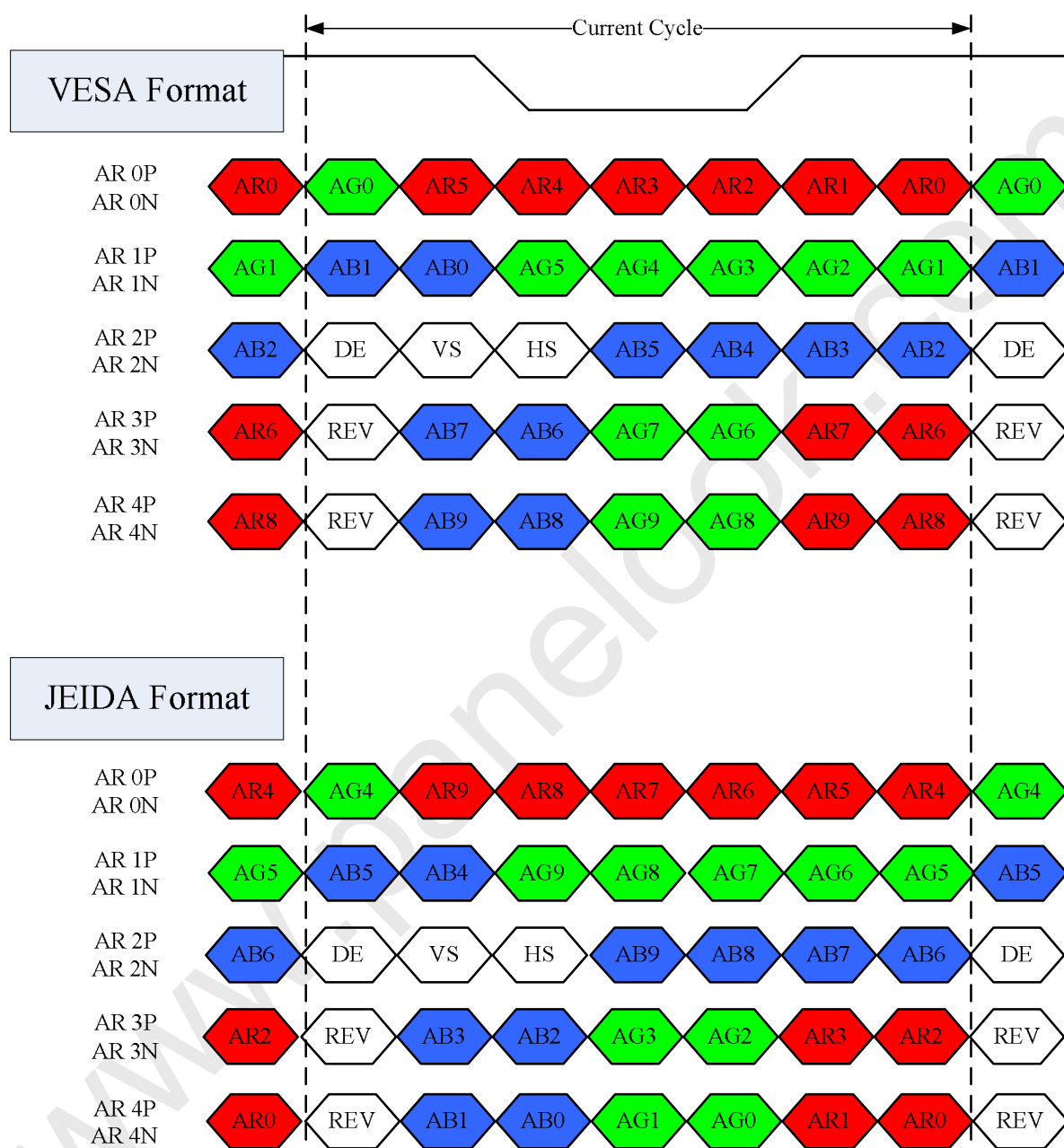
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																															
		Red										Green										Blue											
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:										:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:										:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	

**CHI MEI**
OPTOELECTRONICS CORP.

Issued Date: Mar. 25, 2010

Model No.: V420H2 – LE4

Tentative

Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

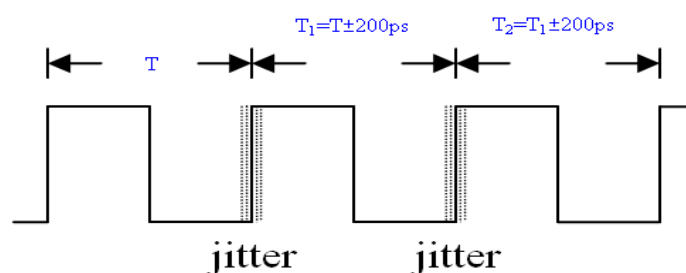
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	78	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	$F_{clkin}-2\%$	—	$F_{clkin}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	30	—	50	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	—	—	ps	(5)
	Hold Time	T_{lvhd}	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	62	Hz	
	Total	T_v	1110	1125	1135	Th	$T_v=T_{vd}+T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	—
	Blank	T_{vb}	30	45	55	Th	—
Horizontal Active Display Term	Total	T_h	1050	1100	1150	Tc	$T_h=T_{hd}+T_{hb}$
	Display	T_{hd}	960	960	960	Tc	—
	Blank	T_{hb}	90	140	190	Tc	—

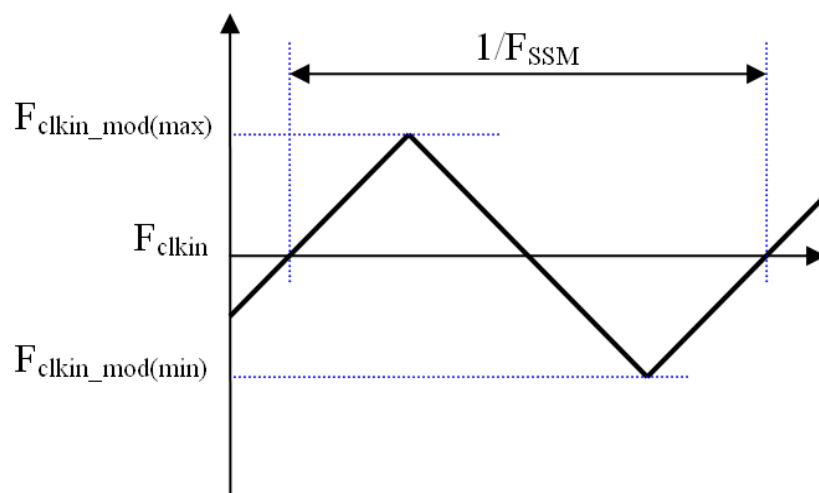
Note (1) Please make sure the range of frame rate has follow the below equation :

$$Fr(max) \geq F_{clkin} \quad / \quad T_v \times T_h \leq Fr(min)$$

Note (2) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$



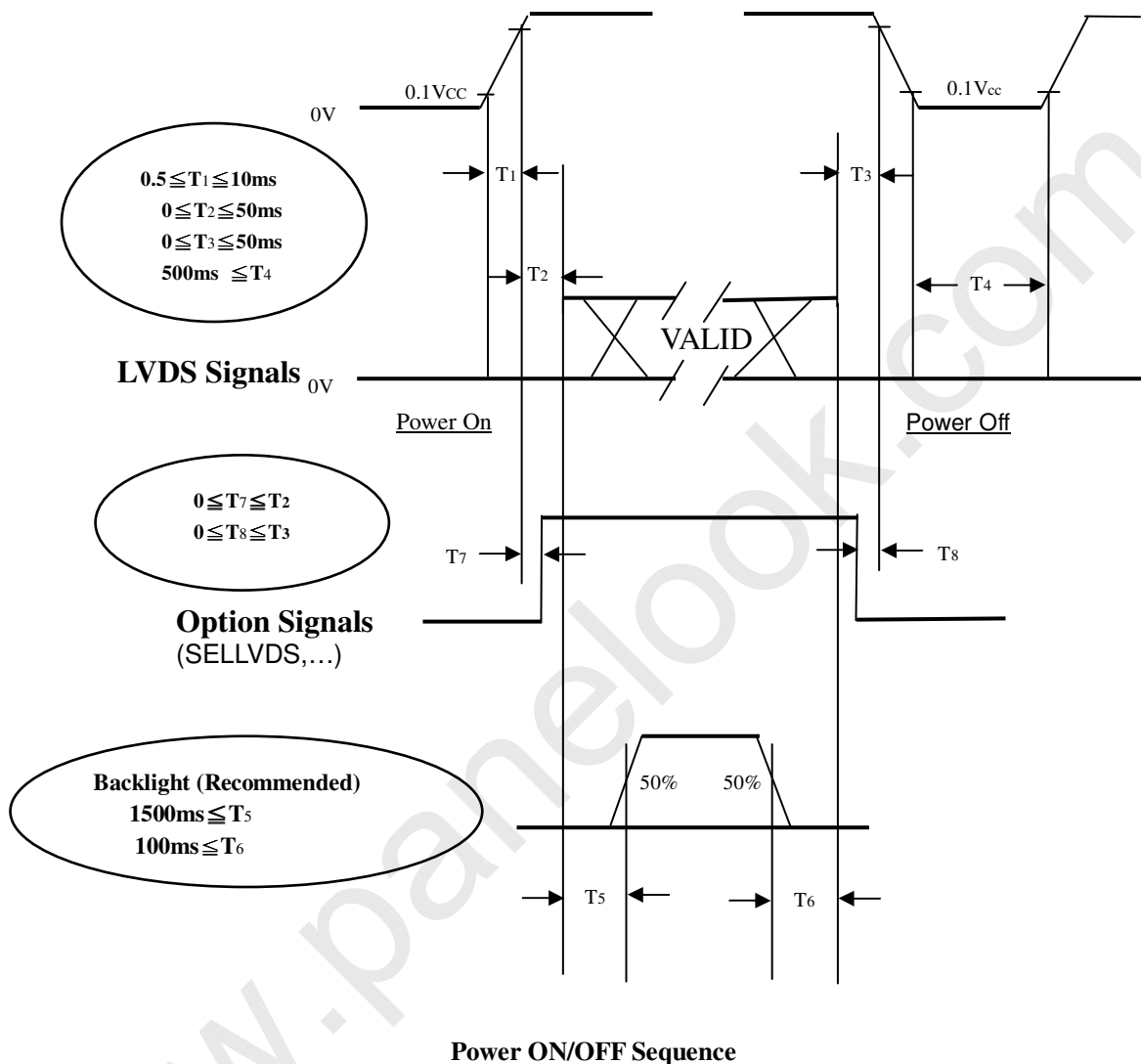
Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

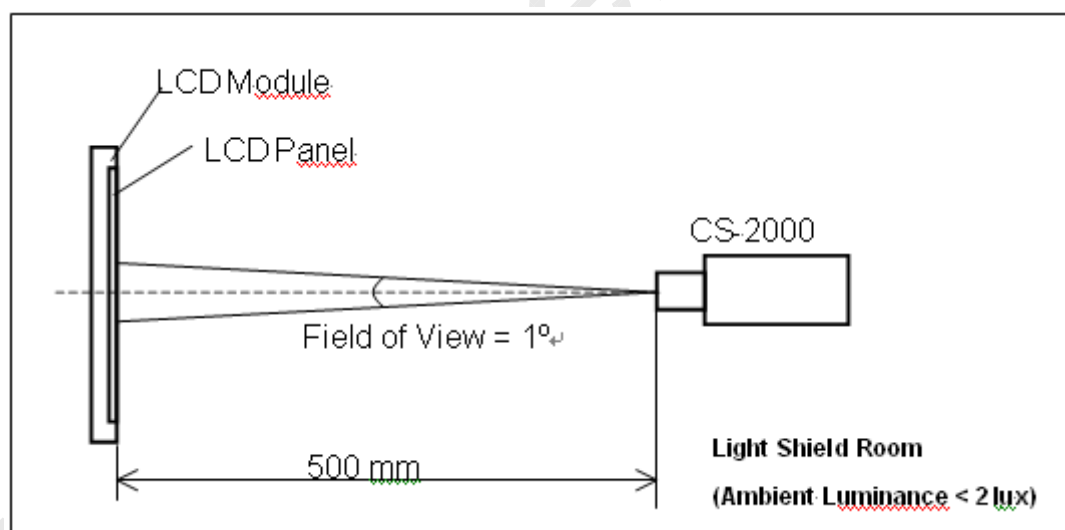
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	80	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



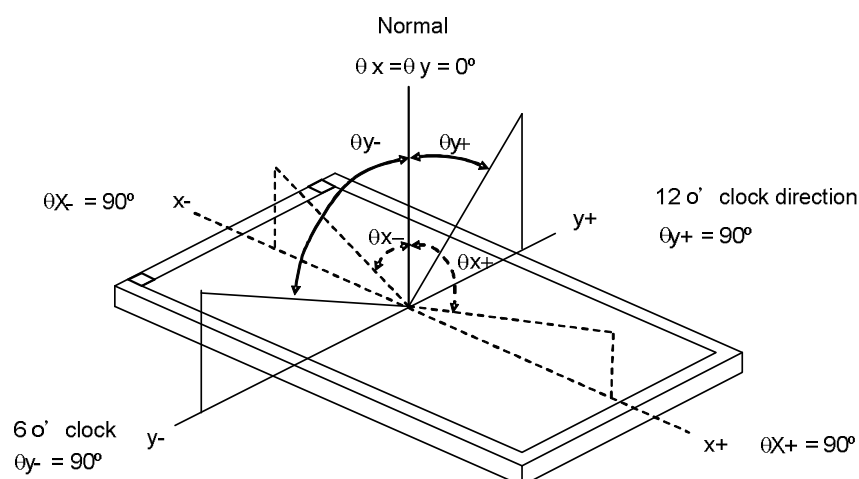
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta x=0^{\circ}$, $\theta y =0^{\circ}$ Viewing angle at normal direction	TBD	(6000)	-	-	Note (2)
Response Time		Gray to gray		-	(5.5)	(11)	ms	Note (3)
Center Luminance of White		LC		(360)	450	-	cd/m ²	Note (4)
White Variation		δW		-	-	(1.3)	-	Note (6)
Cross Talk		CT		-	-	(4)	%	Note (5)
Color Chromaticity	Red	Rx		TBD	TBD	TBD	-	-
		Ry					-	
	Green	Gx					-	
		Gy					-	
	Blue	Bx					-	
		By	-					
	White	Wx	-					
		Wy	-					
	Color Gamut		C.G				--	
Viewing Angle	Horizontal	$\theta x+$	CR \geq 20	80	88	-	Deg.	Note (1)
		$\theta x-$		80	88	-		
	Vertical	$\theta Y+$		80	88	-		
		$\theta Y-$		80	88	-		

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR):

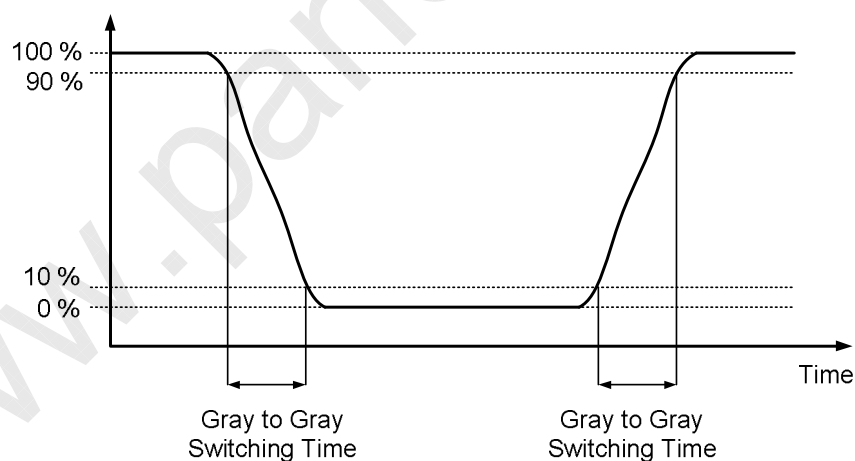
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L (5)$, where $L (X)$ is corresponding to the luminance of the point X at the figure in Note (6).

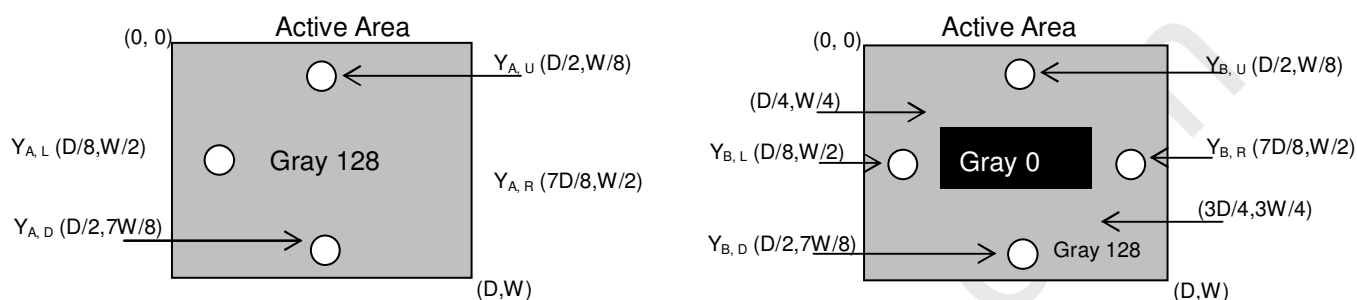
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

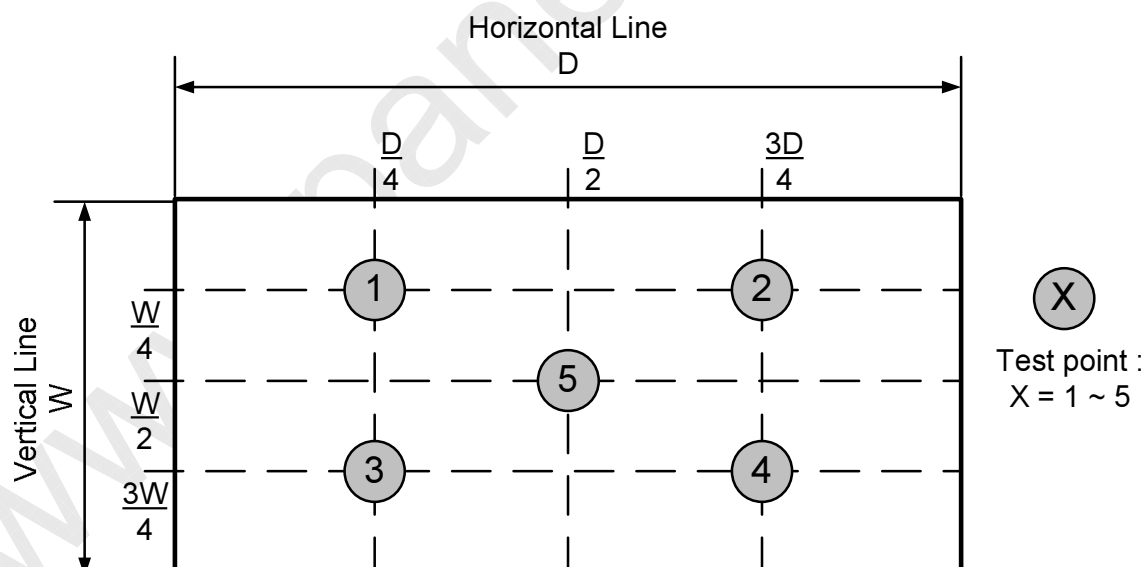
Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

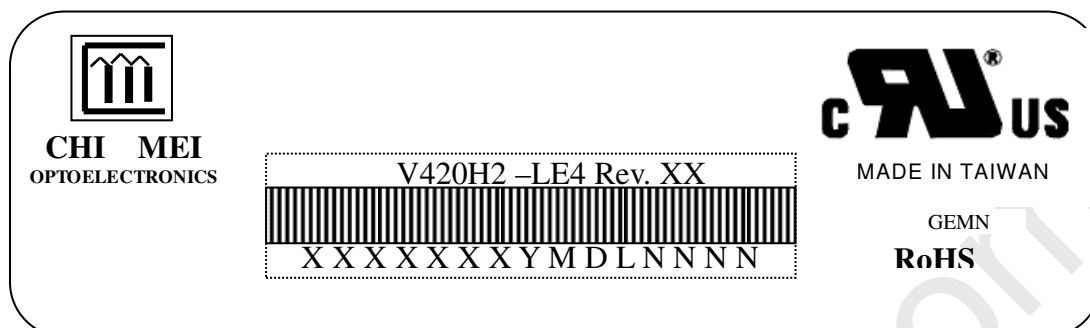
$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

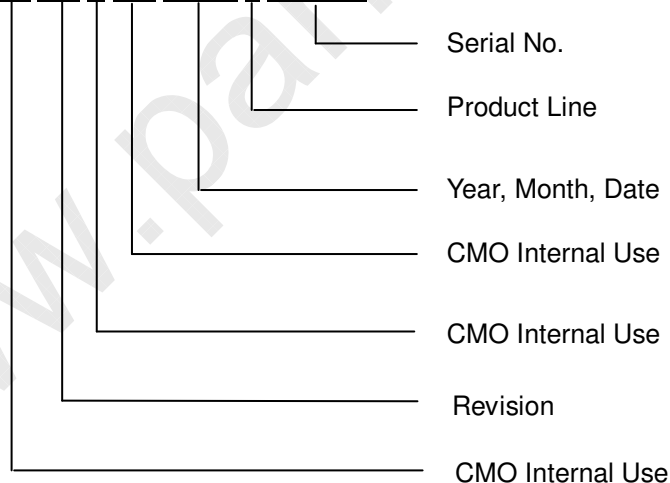
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V420H2-LE4

(b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

(c) Serial ID: XXXXXXYMDLNNNN



Serial ID includes the information as below:

(a) Manufactured Date: Year: 2001=1, 2002=2, 2003=3, 2004=4....2010=0, 2011=1, 2012=2....

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 5 LCD TV modules / 1 Box
- (2) Box dimensions : 1085(L)x296(W)x653(H)mm
- (3) Weight : Approx. TBD Kg(5 modules per carton)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

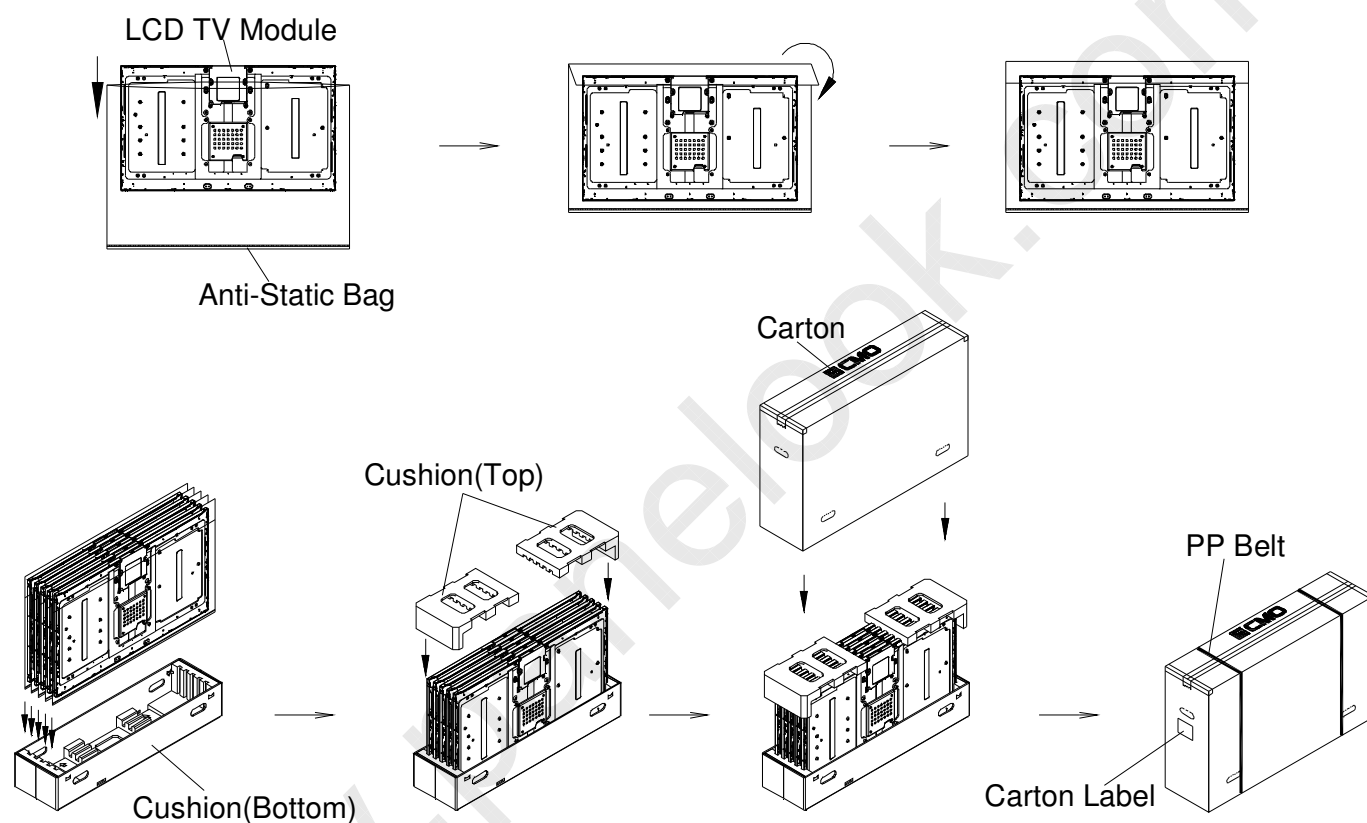


Figure.9-1 packing method



Sea / Land Transportation (40ft Container)

Air Transportation

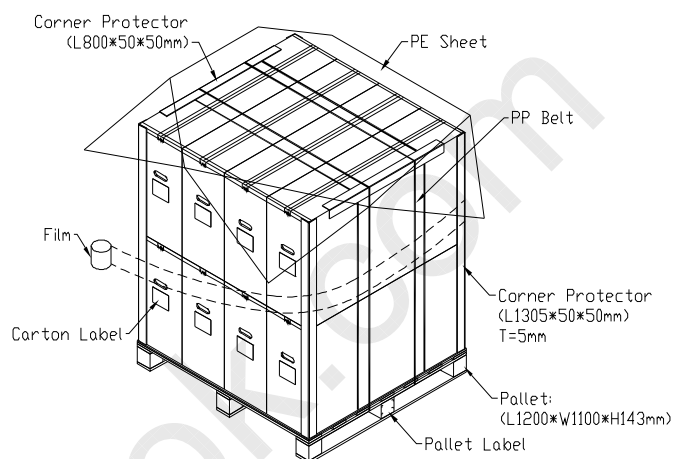
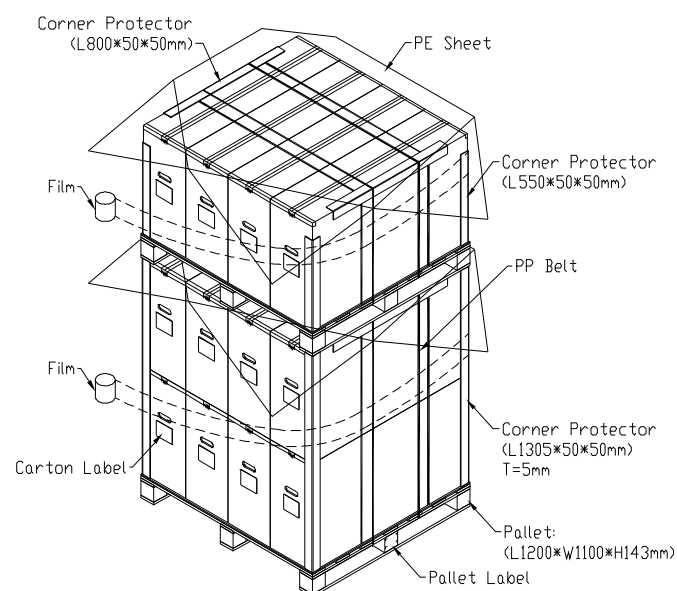


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED light bar will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.



One step solution for LCD / PDP / OLED panel application: Datasheet, inventory and accessory! www.panelook.com



Appendix – TWO Wire BUS INTRODUCTION

A.1 PIN ASSIGNMENT

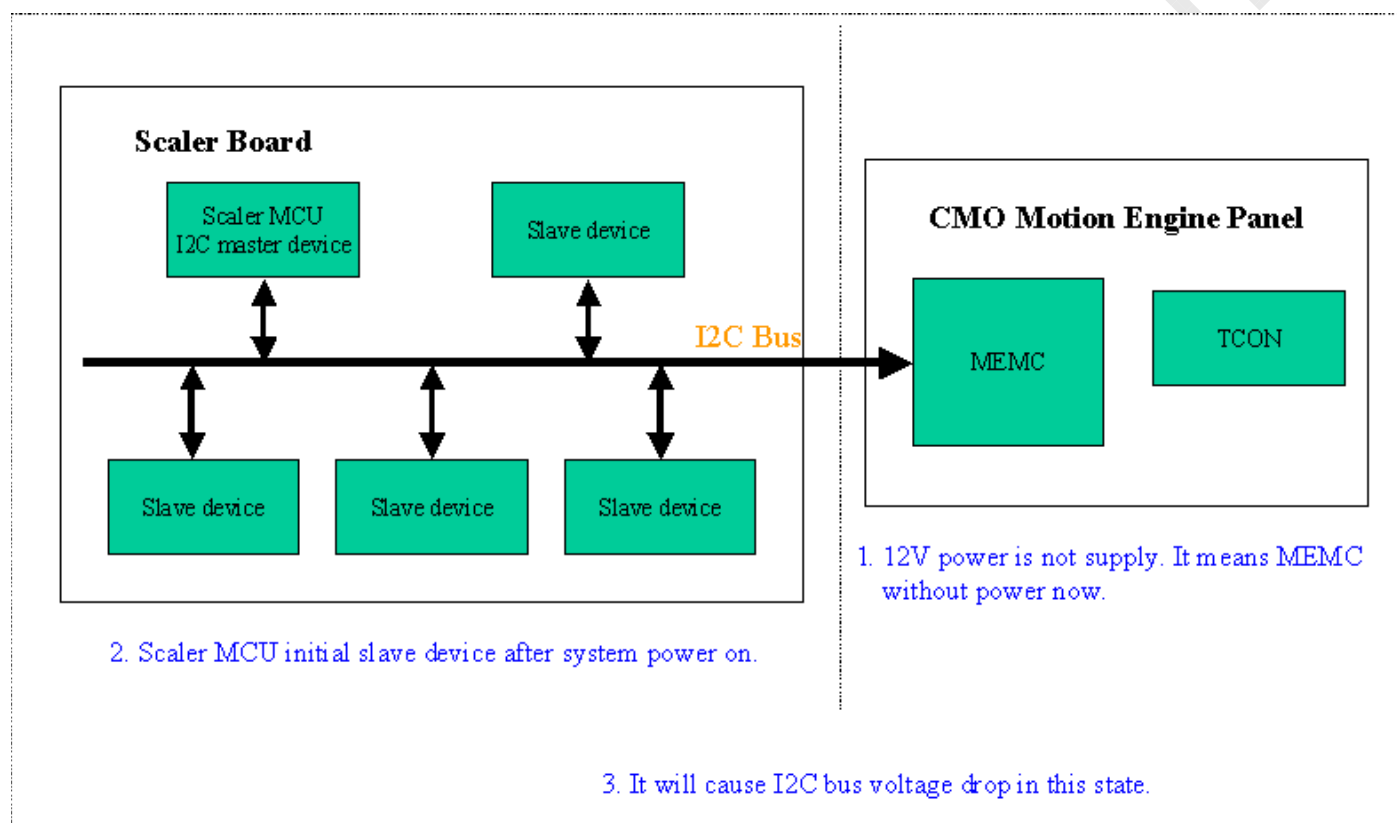
51pins LVDS connector

Pin8: SCL

Pin9: SDA

A.2 I2C BUS APPLICATION NOTE

I2C bus: (The I2C bus must for MEMC only or prevent the I2C bus voltage drop down in initial state)



A.3 TWO WIRE BUS DEVICE ADDRESS

Two wire device address: default is 0x40, 1 byte

Two wire command: the range is 0x00 to 0xFF, 1 byte, see the two wire command table.

Two wire bus format:

Device Address : 0x40 default								Command							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	W/R	L	x	x	x	x	x	x	x

W/R	write : 0; Read : 1
L	1 : 1Byte Data Length; 0: 4Byte Data Length
S	TWI-Bus Start condition from master
Sr	TWI-Bus Start condition from master
A	TWI-Bus Acknowledge bit from master
/A	TWI-Bus Not Acknowledge bit from slave
P	TWI-Bus Stop condition from master
Data	TWI Bus Data from master
Data	TWI Bus Data from slave

A.4 TWO WAY TO CONTROL THE TWO WIRE BUS

There are two options to control the two wires bus command.

Two wire bus 6 bytes format

TWI BUS 6 BYTES FORMATE															
Write Operation															
MSB		LSB		MSB		LSB		MSB						LSB	
S	Device Addr	0	A	0	Command	A	1st Data	A	2nd Data	A	3rd Data	A	4th Data	A	P
1bit	7bit	W	1bit	1bit	7bit	1bit	1bit	1bit	1bit	1bit	1bit	1bit	1bit	1bit	1bit

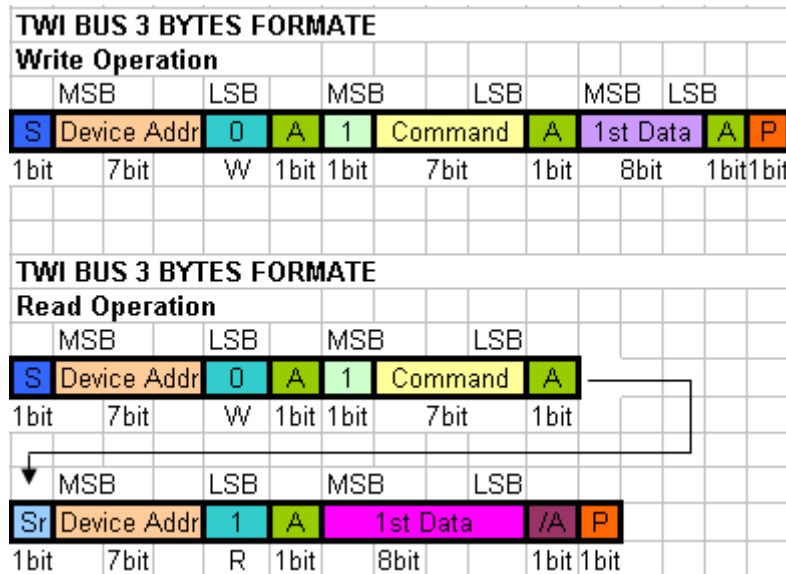
TWI BUS 6 BYTES FORMATE															
Read Operation															
MSB		LSB		MSB		LSB									
S	Device Addr	0	A	0	Command	A									
1bit	7bit	W	1bit	1bit	7bit	1bit									
MSB		LSB		MSB										LSB	
Sr	Device Addr	1	A	1st Data		A	2nd Data	A	3rd Data	A	4th Data	/A	P		
1bit	7bit	R	1bit	8bit		1bit	8bit	1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

Two wire bus 3 bytes format


CHI MEI
 OPTOELECTRONICS CORP.

Issued Date: Mar. 25, 2010

Model No.: V420H2 – LE4

Tentative


Note:

A transmission basically consists of a START condition, a SLA+R/W, one or more data packets and a STOP condition. An empty message, consisting of a START followed by a STOP condition, is illegal. Note that the wired-ANDing of the SCL line can be used to implement handshaking between the master and the slave. The slave can extend the SCL low period by pulling the SCL line low. This is useful if the clock speed set up by the master is too fast for the slave, or the slave needs extra time for processing between the data transmissions. The slave extending the SCL low period will not affect the SCL high period, which is determined by the master. As a consequence, the slave can reduce the TWI data transfer speed by prolonging the SCL duty cycle.

A.5 TWO WIRE BUS COMMAND TABLE

There is two wire bus command table.

Command Name		Access Mode	Description
All OSD Protection	0x00	R/W	OSDx Enable Flag Contorl
OSD1_Start_Protection	0x01	R/W	OSD1 Protection Start Position
OSD2_Start_Protection	0x02	R/W	OSD2 Protection Start Position
OSD3_Start_Protection	0x03	R/W	OSD3 Protection Start Position
OSD4_Start_Protection	0x04	R/W	OSD4 Protection Start Position
OSD1_End_Protection	0x05	R/W	OSD1 Protection End Position
OSD2_End_Protection	0x06	R/W	OSD2 Protection End Position
OSD3_End_Protection	0x07	R/W	OSD3 Protection End Position
OSD4_End_Protection	0x08	R/W	OSD4 Protection End Position
Demo Window	0x09	R/W	ME Performance Demo
MEMC Level	0x0A	R/W	ME Performance
GV Mode	0x0B	R/W	ME Operation
Blanking	0x0C	R/W	Blinking the screen
RPF	0x0D	R/W	Rotation picture function

(x1, y1)

OSD protection is rectangle. Please locate the position as below,
 (x1-Left, y1-Top) (x2-Right, y2-Bottom)

Motion engine is not active in this blue area.

(x2, y2)

Enable All OSD Protection

AllOSD Protection : 0x00															
4 Bytes Data Length															
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24					D31~D28	Unused	
	Unused				OSDx								D27	OSD4 flag 1 : On ; 0 : Off	
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16					D26	OSD3 flag 1 : On ; 0 : Off	
	Unused												D25	OSD2 flag 1 : On ; 0 : Off	
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8					D24	OSD1 flag 1 : On ; 0 : Off	
	Unused												D23~D0	Unused	
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0							
	Unused														
AllOSD Protection : 0x80															
1 Byte Data Length															
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0					D7~D4	Unused	
	Unused				OSDx								D3	OSD4 flag 1 : On ; 0 : Off	
													D2	OSD3 flag 1 : On ; 0 : Off	
													D1	OSD2 flag 1 : On ; 0 : Off	
													D0	OSD1 flag 1 : On ; 0 : Off	

OSD # 1~4 Start Protection

OSD1_Start_Protection : 0x01															
OSD2_Start_Protection : 0x02															
OSD3_Start_Protection : 0x03															
OSD4_Start_Protection : 0x04															
4 Bytes Data Length															
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31		OSDx flag 1 : On ; 0 : Off				
			Unused							D30~D27		Unused			
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D26~D16		OSDx Left position				
	OSD Left										D15~D11		Unused		
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8	D10~D0		OSDx Top position				
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0							
	OSDx Top														
										Left position Max : 1919					
										Top position Max : 1079					

OSD # 1~4 End Protection

OSD1_End_Protection : 0x05															
OSD2_End_Protection : 0x06															
OSD3_End_Protection : 0x07															
OSD4_End_Protection : 0x08															
4 Bytes Data Length															
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	<div>D31~D27Unused</div> <div>D26~D16OSDx Right position</div> <div>D15~D11Unused</div> <div>D10~D0OSDx Bottom position</div> <div>Right position Max : 1919</div> <div>Bottom position Max : 1079</div>						
	Unused														
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16							
	OSD Right														
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8							
	Unused														
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0							
	OSD Bottom														

Demo Window

Demo Window : 0x09																	
4 Bytes Data Length																	
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D25		Unused						
	Unused								D24	Demo Window 1 : On ; 0 : Off							
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0		Unused						
	Unused																
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8									
	Unused																
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0									
	Unused																
Demo Window : 0x89																	
1 Byte Data Length																	
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1		Unused						
	Unused								D0	Demo Window 1 : On ; 0 : Off							

MEMC Level

ME Level : 0x0A															
4 Bytes Data Length															
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D29		Unused				
	Unused				ME Level				D28~24		ME Level 0~F				
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16			0 : Off 3 : Weak 8 : Normal D : Strong				
	Unused														
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8							
	Unused														
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0							
	Unused														
									D23~D0		Unused				
ME Level : 0x8A															
1 Byte Data Length															
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D4		Unused				
	Unused				ME Level				D3~D0		ME Level 0~F				
											0 : Off 3 : Weak 8 : Normal D : Strong				

GV Mode

GV Mode : 0x0B															
4 Bytes Data Length															
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24					D31~D25	Unused	
	Unused							D24					1 : Graphic ; 0 : Video		
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16					D23~D0	Unused	
	Unused														
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9	D8							
	Unused														
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0							
	Unused														
GV Mode : 0x8B															
1 Byte Data Length															
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0			D7~D1	Unused			
	Unused							D0			1 : Graphic ; 0 : Video				

Blanking (Enable/Disable)

Blanking : 0x0C																		
4 Bytes Data Length																		
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D26		Unused							
	Unused								D24		Blanking; 1 : On ; 0 : Off							
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0		Unused							
	Unused							When the input signal is unstable, the screen should be blanked.										
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9									D8		
	Unused																	
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1									D0		
	Unused																	
Blanking : 0x8C																		
1 Byte Data Length																		
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1		Unused							
	Unused								D0		Blanking; 1 : On ; 0 : Off							

Rotation Panel Function

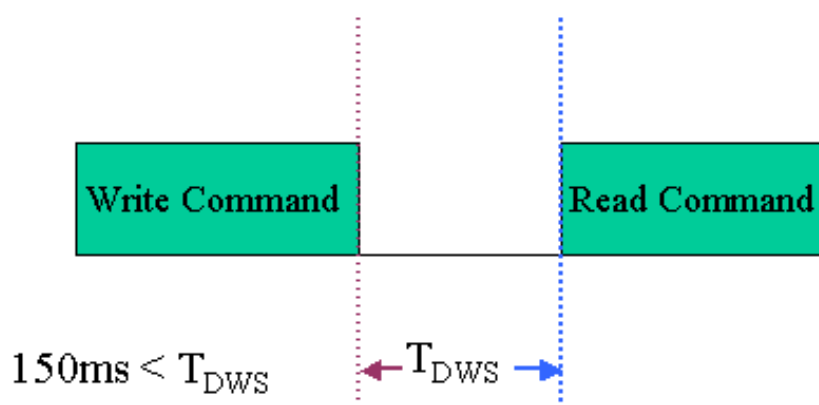
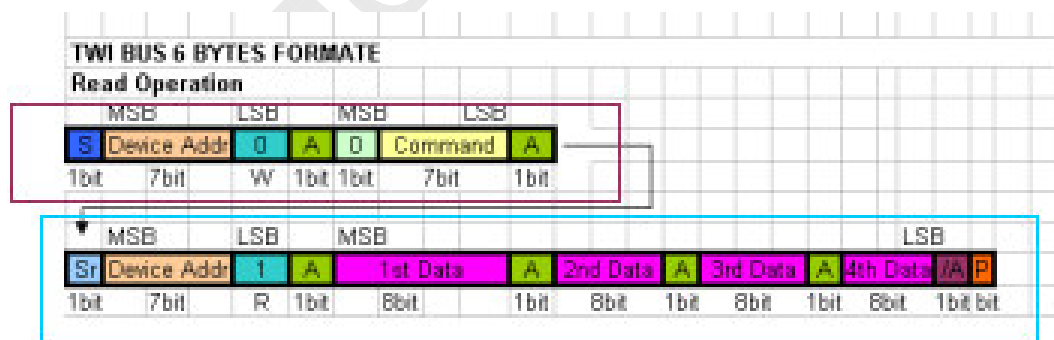
RPF : 0x0D																
4 Bytes Data Length																
1st BYTE DATA	D31	D30	D29	D28	D27	D26	D25	D24	D31~D26	Unused						
	Unused							D24	Rotation; 1 : 180°; 0 : 0°							
2nd BYTE DATA	D23	D22	D21	D20	D19	D18	D17	D16	D23~D0	Unused						
	Unused							D: Normal display ↓ 1: Rotation display ↗								
3rd BYTE DATA	D15	D14	D13	D12	D11	D10	D9									D8
	Unused															
4th BYTE DATA	D7	D6	D5	D4	D3	D2	D1									D0
	Unused															
RPF : 0x8D																
1 Byte Data Length																
1st BYTE DATA	D7	D6	D5	D4	D3	D2	D1	D0	D7~D1	Unused						
	Unused							D0	Rotation; 1 : 180°; 0 : 0°							

A.6 TWO WIRE BUS REQUIREMENT

Symbol	Parameter	Condition	Min	Max	Unit
V_L	Input Low-voltage		0	0.7	V
V_H	Input High-voltage		2.7	3.3	V
t_r	Rise Time for both SDA and SCL		$20 + 0.1C_b$	300	ns
t_{cf}	Output Fall Time from V_{IHmin} to V_{ILmax}	$10\text{ pF} < C_b < 400\text{ pF}$	$20 + 0.1C_b$	250	ns
I_i	Input Current each I/O Pin	$0.1V_{CC} < V_i < 0.9V_{CC}$	-10	10	uA
C_i	Capacitance for each I/O Pin		NA	10	pF
f_{SCL}	SCL Clock Frequency		4	50	KHz
R_P	Value of Pull-up resistor	$f_{SCL} \leq 50\text{KHz}$	3000	$1000\text{ns}/C_b$	Ω
t_{HDSTA}	Hold Time (repeated) STAR Condition	$f_{SCL} \leq 50\text{KHz}$	4	NA	us
t_{LOW}	Low Period of the SCL Clock	$f_{SCL} \leq 50\text{KHz}$	4.7	NA	us
t_{HIGH}	High Period of the SCL Clock	$f_{SCL} \leq 50\text{KHz}$	4	NA	us
t_{SUSTA}	Set-up time for a repeated STAR Condition	$f_{SCL} \leq 50\text{KHz}$	4.7	NA	us
t_{HDDAT}	Data hold time	$f_{SCL} \leq 50\text{KHz}$	0	3.45	us
t_{SUDAT}	Data setup time	$f_{SCL} \leq 50\text{KHz}$	250	NA	ns
t_{SUSTO}	Setup time for STOP Condition	$f_{SCL} \leq 50\text{KHz}$	4	NA	us
t_{QLF}	Bus free time between a STOP and START Condition	$f_{SCL} \leq 50\text{KHz}$	4.7	NA	us

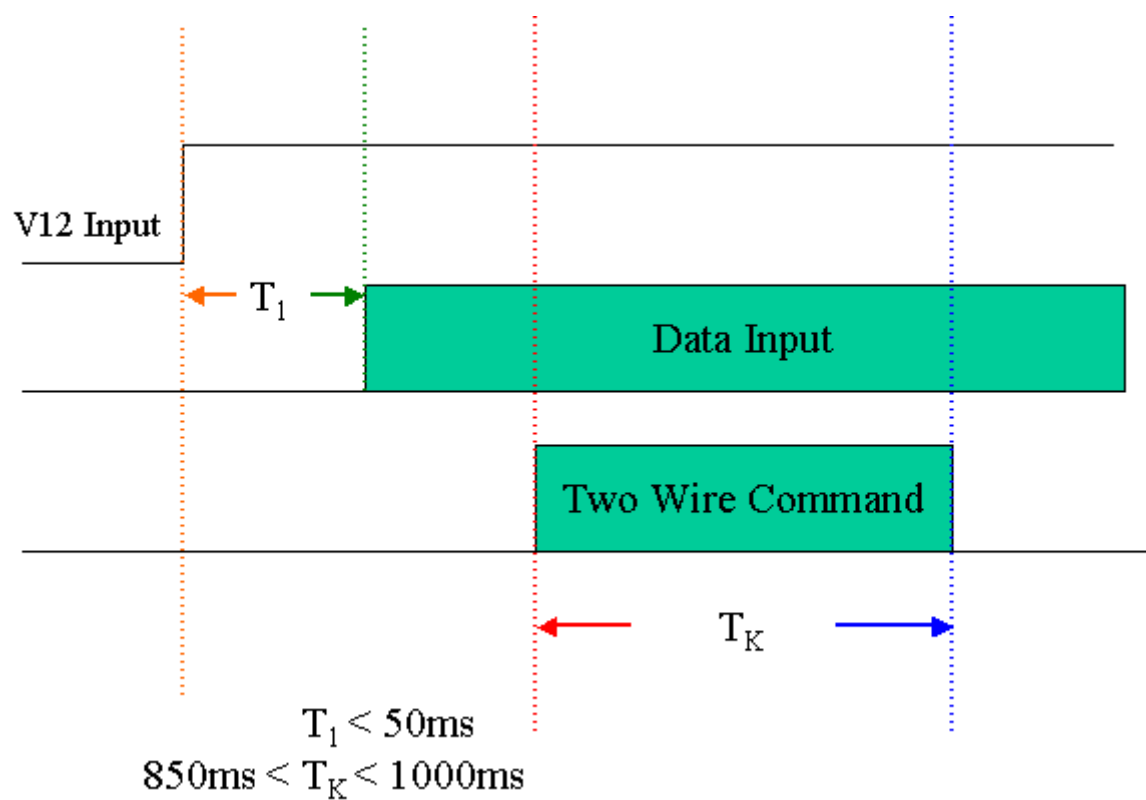
Write Command

Read Command



A.7 THE TWO WIRE BUS SEQUENCE

I. Initial state



II. Stable state

